Please replace the paragraph beginning at page 8, line 24, with the following rewritten paragraph:

The section shape of the reflected light is a regular circle when the light beam is focused on a pit, and is elliptical when not focused on a pit. Each of the four focus detector sensors output the same detection signal when the reflected beam is circular, and output different detection signals when the reflected beam is elliptical. Assuming that sensors A and B detect the reflected light lopsided toward the inside circumference of the track and sensors C and D detect the reflected light lopsided toward the outside circumference of the track. The output signal of sensor A is denoted as "A", and the like, and a TE signal can obtained by (A+B)-(C+D).

Please replace the paragraph beginning at page 9, line 24, with the following rewritten paragraph:

As will be known from Fig. 2, grooves 33 and lands 34 wobble in a sine wave pattern orthogonally to the track trace. An advantage of this is that recording time can be shortened by detecting the period of this sine wave wobble signal, generating a clock synchronized to the detection signal, and writing data synchronized to this clock. This is because wobble appears substantially continuously in one rotation of grooves 33 and lands 34, and a wobble PLL circuit for generating recording clocks (not shown) can therefore quickly lock onto the phase.

Please replace the paragraph beginning at page 11, line 1, with the following rewritten paragraph:

As shown in (h) in Fig. 3, header area 81, identified by IDa in Fig. 2, contains VFO 83a, address ID 83b, VFO 84a, and address ID 84b. Header area 81 likewise contains VFO 85a, address ID 85b, VFO 86a, and address ID 86b.

Please replace the paragraph beginning at page 11, line 7, with the following rewritten paragraph:

The read signal from optical disc 1 generated by optical pickup 2 is input to preamplifier 3. Preamplifier 3 outputs an RF signal ((a) in Fig. 3) and TE signal ((b) in Fig. 3). As shown in the

Figure, these signals have a high level (= 1) signal level when header area 81 is read. This is because header area 81 is manufactured with high reflectivity. The RF signal is input to clamping unit 4 and amplitude fluctuation detector 14. The TE signal is input to clamping unit 4, wobble dropout detector 16, and wobble digitizer 19.

Please replace the paragraph beginning at page 12, line 23, with the following rewritten paragraph:

The read gate signal ((e) in Fig. 3) goes between the high level and low level three times in one sector. That is, the read gate signal rises slightly delayed from the start of VFO 83a and 85a, falls at the end of address information 84b and 86b, rises slightly delayed from the beginning of VFO 88, and falls in second guard area 90. Note that approximately the center of the amplitude variation of output signal from clamping unit 4 shown in (c) in Fig. 3 is matched to voltage Vcen.

Please replace the paragraph beginning at page 13, line 5, with the following rewritten paragraph:

Referring again to Fig. 1, wobble digitizer 19 outputs a binary wobble signal ((f) in Fig. 3) to PLL circuit 12. PLL circuit 12 controls frequency by counting and comparing the period of this binary wobble signal with its own clock. As shown in Fig. 1, PLL circuit 12 also receives the read gate signal from controller 13 and performs feedback control so as to synchronize with a predetermined reference phase. When the feedback signal synchronizes with the reference phase, PLL circuit 12 locks the phase of the feedback signal. An RF signal output from A/D converter 8 and sampled at the output clock of PLL circuit 12 is input to PLL circuit 12. When the frequency enters the capture range as a result of the above-noted frequency control, PLL circuit 12 applies phase control and sets the zero cross point sample value to zero. PLL circuit 12 also generates and supplies to other components a clock synchronized to the RF signal. Signal processor 11 applies Viterbi decoding, demodulation, or other process, and outputs address information and user data to controller 13 and other downstream circuits (not shown in the Figure).

Please replace the paragraph beginning at page 15, line 12, with the following rewritten paragraph:

Amplitude fluctuation detector 14 detects the upper envelope, which is the output when the RF signal reflection is bright, and slices the envelope signal at a fixed level. Parts lower than the slice level are output as a "1", and higher parts are output as a "0" ((m) in Fig. 5). This means that output goes high level (= 1) when the black dot is read, and then goes low level (= 0) after the black dot is passed. Wobble dropout detector 16 full-wave rectifies the TE signal. That is, wobble dropout detector 16 inverts signals below a specific reference level to a signal level above this reference level to generate a full-wave rectified signal. Wobble dropout detector 16 slices this full-wave rectified signal at a fixed level, and outputs parts below the slice level high level (= 1) and parts above the slice level low level (= 0) ((q) in Fig. 5). As with output from amplitude fluctuation detector 14, output goes to the high level (= 1) when the black dot is read, and then goes to the low level (= 0) after passing the black dot.

Please replace the paragraph beginning at page 17, line 6, with the following rewritten paragraph:

First, data is read from optical disc 1 (Fig. 1) to generate an RF signal (step S602). This RF signal is shown in (j) in Fig. 5. When the RF signal is obtained, controller 13 (Fig. 1) instructs selector 18 (Fig. 1) to select a low level signal and determines whether reproduction (reading) is possible using that RF signal (step S604). This low level signal is a null signal without valid polarity, and means that clamping is not applied. Null signal selection is possible because there are cases, such as when fine amplitude variation continues for an extended time due to, such as, fingerprints, when reading is easier if clamping is not applied even though amplitude variation is detected. If the null signal is selected, the waveform of the output signal from clamping unit 4 (Fig. 1) is as shown in (k) in Fig. 5. When a signal such as this is output from clamping unit 4 (Fig. 1) and as a result, reproduction is possible, control skips to the subsequent signal processing operation (step S616) of the signal processor 11 (Fig. 1).

Please replace the paragraph beginning at page 17, line 20, with the following rewritten paragraph:

However, as previously described with reference to (t) in Fig. 5, if the output signal from clamping unit 4 is input to A/D converter 8 and this input signal exceeds the reference level of A/D converter 8, that part of the signal above the reference level cannot be reproduced. In this case, the same selection signal (that is, a null signal) is output again (step S606). This is because the first reproduction attempt may simply fail accidentally.

Please replace the paragraph beginning at page 20, line 19, with the following rewritten paragraph:

The functions of the new elements noted in (3) above are described below. Output signal from equalizer 6 and the digital voltage signal from digital voltage generator 42 are input to comparator 41 and second differential amplifier 43. Comparator 41 compares the output signal from equalizer 6 and the output signal from digital voltage generator 42. If the output signal from equalizer 6 is greater, comparator output signal s goes to the high level (= 1), and otherwise goes to the low level (= 0). Comparator 41 also outputs the inversion t of output signal s. Both output signals s and t are input to digital voltage generator 42. Digital voltage generator 42 is provided to maintain the duty ratio between 1s and 0s in the comparator 41 output signals to a specific value (such as 1 in this example) based on the read gate signal from controller 13. More specifically, digital voltage generator 42 outputs the difference between output signal s and inverse signal t from comparator 41. The output signal from digital voltage generator 42 is input to second differential amplifier 43 and as feedback to the comparator 41. Second differential amplifier 43 outputs the difference of the digital voltage output signal from digital voltage generator 42 subtracted from the output signal from equalizer 6.

Please replace the paragraph beginning at page 21, line 11, with the following rewritten paragraph:

Fig. 8 shows the configuration of digital voltage generator 42 in detail. Digital voltage generator 42 has a differential amplifier 421, analog switch 422, resistor Rc 423, resistor Rd 424,

inverting integrator 425, and inverting amplifier 426. Differential amplifier 421 compares output signals s and t from comparator 41 (Fig. 7), outputs high level (= 1) if output signal s is higher, and outputs low level (= 0) if output signal s is lower. Analog switch 422 switches the circuit according to whether the read gate signal is 0 or 1. That is, analog switch 422 closes to resistor Rc 423 when the read gate signal is high level (= 1), and closes to resistor Rd 424 when the read gate signal is low level (= 0). Note that Rd is here sufficiently low compared with Rc. For example, preferably Rd ≈ Rc/10. This ensures rapid signal tracking when the read gate signal is low level (= 0) because the signal passes the sufficiently low resistor Rd 424. Signals passing resistor Rc 423 or resistor Rd 424 are sequentially input to the series connected inverting integrator 425 and inverting amplifier 426. Inverting integrator 425 and inverting amplifier 426 charge the high level difference between output signals s and t from comparator 41 (Fig. 7) and a specific reference level to the capacitor of inverting integrator 425, and also output the difference.

A12

IN THE CLAIMS

Please amend claims 2 and 5-7 as follows.

A13

2. (Amended) An optical disc apparatus as described in claim 1, further comprising a controller which generates a control signal instructing which signal to select,

wherein the selection unit selects a signal based on the control signal generated by the controller.

A14

5. (Amended) An optical disc apparatus as described in claim 4, further comprising at least one additional one of the detection signal generator; and

an amplitude fluctuation signal delay unit which delays the amplitude fluctuation signal generated by the amplitude fluctuation sensing unit, and generates an extended amplitude fluctuation signal extended by a delay period,

wherein the controller generates a control signal instructing selection of the extended amplitude fluctuation signal when a read error occurs after generating a control signal instructing selection of the amplitude fluctuation signal.

6. (Amended) An optical disc apparatus as described in claim 5 wherein a recording guide groove wobbling at a specific period is formed on the optical disc, the optical disc apparatus further comprising:

a dropout detection unit which detects dropout of a wobble signal corresponding to the guide groove period when reading the optical disc, and generates a dropout detection signal; and

a signal delay unit which delays the dropout detection signal generated by the dropout detection unit, and generates an extended dropout detection signal that is extended for a delay period,

wherein the controller additionally generates a control signal instructing selection of the dropout detection signal, and generates a control signal instructing selection of the extended dropout detection signal when a read error occurs.

7. (Amended) An optical disc apparatus for applying a specific signal process to a playback signal read from an optical disc, the optical disc apparatus comprising:

a digitizing unit which digitizes the playback signal and outputs a digital playback signal;

a digital voltage generator which forms a feedback loop with the digitizing unit to output a voltage signal such that a duty ratio of the digitized playback signal from the digitizing unit is a specific value;

a differential amplifier which outputs a differential signal between the playback signal and the voltage signal of the digital voltage generator; and

a signal processing unit which performs a specific signal process based on the differential signal from the differential amplifier.